# Title:

Study of different Flip-Flops.

# Objective:

The experiment aims to understand the operation and characteristics of different types of flip-flops (D, J-K, and T flip-flops), focusing on their functionality and behavior with clock inputs.

# Theory:

Flip-flops are fundamental elements in digital electronics, specifically in sequential logic circuits, and they serve as memory devices to store a single bit of data. Flip-flops change their output based on a clock signal, and they have various configurations depending on how they are designed to respond to input signals.

1. **D Flip-Flop:**
   * The **D Flip-Flop** (Data or Delay Flip-Flop) has one control input, D, and a clock input. The output, Q, follows the D input, but only at the positive edge of the clock signal. Once Q captures the value of D at the clock's positive edge, it holds that value until the next positive clock edge, regardless of any further changes to D. Some D flip-flops also have **Preset** and **Clear** inputs to force the output to 1 or 0, respectively.

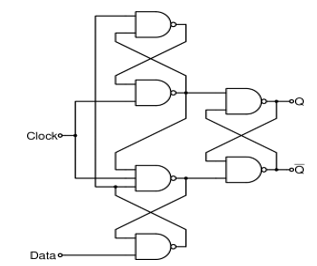


Figure - D FLIP-FLOP LOGICAL CIRCUIT

Figure -

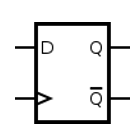


Figure 2 - D FLIP-FLOP GRAPHICAL SYMBOL

1. **J-K Flip-Flop:**
   * The **J-K Flip-Flop** has two control inputs, J and K. When J = 1 and K = 0, the output Q is set to 1. When J = 0 and K = 1, Q is reset to 0. If both J and K are 0, the output remains unchanged. When both J and K are 1, the output toggles between 0 and 1 with each clock pulse. This flip-flop is an improvement over the simpler SR flip-flop, as it resolves the invalid state that occurs when both inputs are 1.

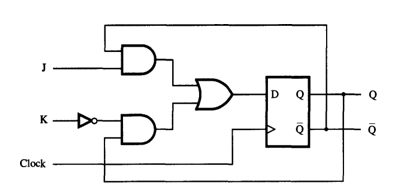


Figure - J-K FLIP-FLOP USING D FLIP-FLOP

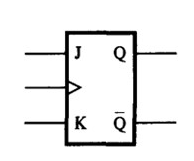


Figure - J-K FLIP-FLOP GRAPHICAL SYMBOL

1. **T Flip-Flop:**
   * The **T Flip-Flop** (Toggle Flip-Flop) is a variation of the J-K flip-flop where both the J and K inputs are tied together, making it a single input labeled T. When T = 1, the output toggles between 0 and 1 at each positive clock edge. If T = 0, the output remains unchanged.

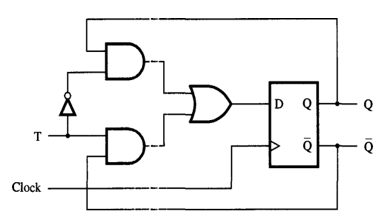


Figure - T FLIP-FLOP USING D FLIP-FLOP

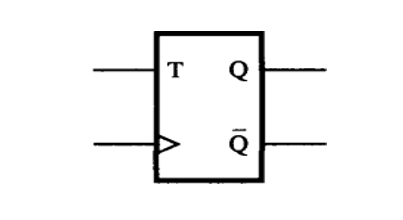


Figure - GRAPHICAL SYMBOL OF T FLIP-FLOP

1. **Clock Signals:**
   * Flip-flops are **edge-triggered**, meaning they respond only to the rising (positive) or falling (negative) edge of a clock signal. The clock ensures synchronization in sequential circuits, allowing data changes to occur only at specific intervals.
2. **Outputs (Q and Q'):**
   * Each flip-flop has two outputs: Q (the stored bit) and Q' (the complement of Q). The state of Q represents the current value being held by the flip-flop, while Q' is its inverse.
3. **Applications:**
   * Flip-flops are widely used in memory elements, registers, counters, and various types of state machines within digital circuits.

# Apparatus:

* IC 7404 (NOT Gate) – 1 piece
* IC 7408 (AND Gate) – 2 pieces
* IC 7432 (OR Gate) – 1 piece
* IC 7400 (NAND Gate) – 6 pieces
* IC 7474 (D Flip-Flop) – 1 piece
* IC 7476 (J-K Flip-Flop) – 1 piece
* Trainer board
* Pulse switch (for clock generation)
* Power supply
* Connecting wires

# Experimental Procedure:

1. **Setup:**

* Gather all necessary components: IC 7474 (D flip-flop), IC 7476 (J-K flip-flop), 7404 (NOT gate), 7408 (AND gate), 7432 (OR gate), and 7400 (NAND gate).
* Mount the ICs on a breadboard or trainer board and connect the appropriate power supply.

1. **D Flip-Flop:**

* Connect the circuit for a positive edge-triggered D flip-flop.
* Use a pulse switch to generate clock signals.
* Observe how the output Q changes only when the clock reaches a positive edge, regardless of any changes in the D input during the clock cycle.
* Record the timing diagram for the D flip-flop showing input D, clock, and output Q.

1. **J-K Flip-Flop:**

* Implement the circuit for a positive edge-triggered J-K flip-flop.
* Set different values for J and K (00, 01, 10, and 11) and observe how the output changes or remains constant depending on the input values at the positive clock edge.
* Create the timing diagram to represent the behavior of the J-K flip-flop under different input combinations.

1. **T Flip-Flop:**

* Connect the circuit for a T flip-flop by shorting the J and K inputs of the J-K flip-flop.
* Observe how the output toggles between 0 and 1 only when T = 1 at each positive clock edge.
* Record the timing diagram for the T flip-flop showing the clock, T input, and Q output.

1. **Clear and Preset Inputs:**

* If available in the design, activate the **Preset** and **Clear** inputs for the D flip-flop and observe how the outputs behave.
* The **Preset** input forces Q = 1, while the **Clear** input forces Q = 0, regardless of the clock or other inputs.

1. **Measurement:**

* For each flip-flop, ensure to observe how the outputs react to changes in the clock and input signals.
* Generate accurate timing diagrams for each flip-flop based on the experimental observations.

1. **Precaution:**

* Ensure that **Preset** and **Clear** are not activated simultaneously, as this may lead to erroneous results or damage to the IC.

# Results:

The Multisim simulation for the different types of Flip-flops are shown below.

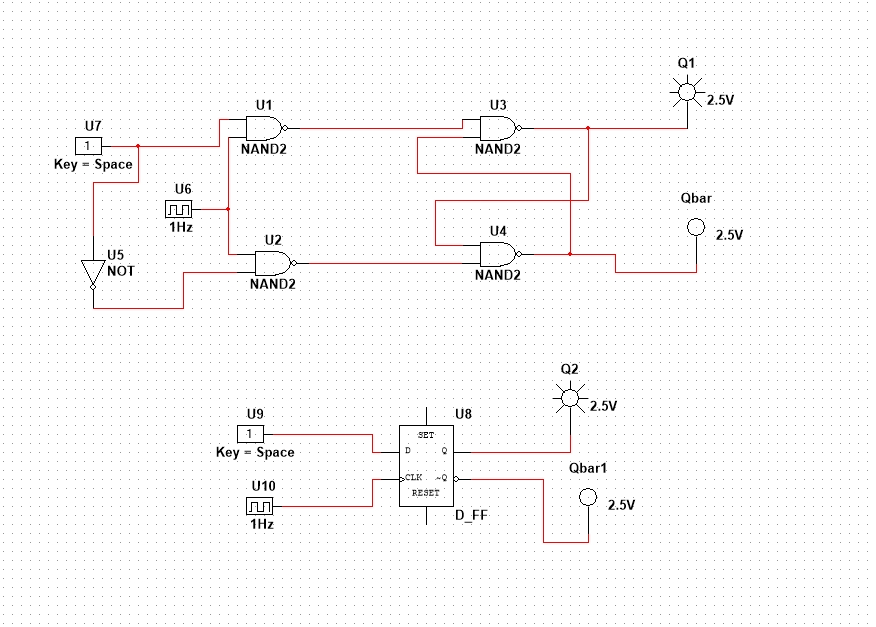


Figure - D FLIP-FLOP

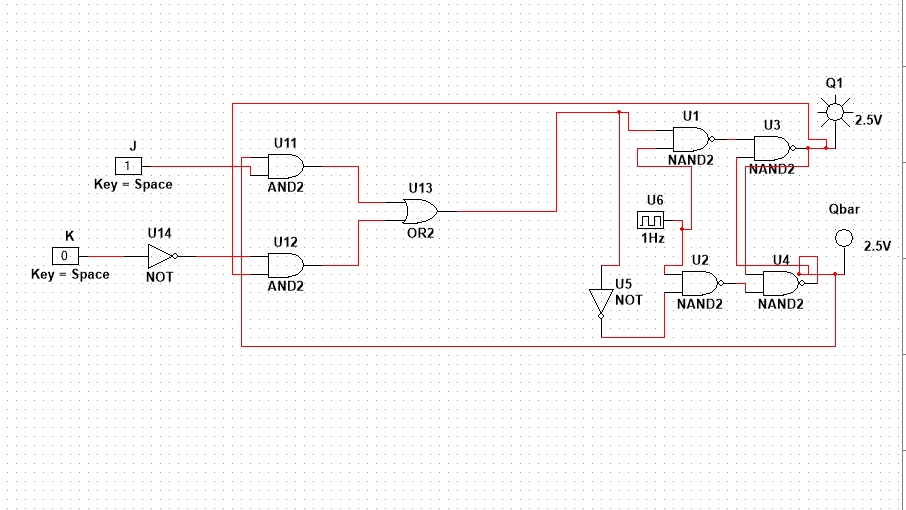


Figure - J-K FLIP-FLOP

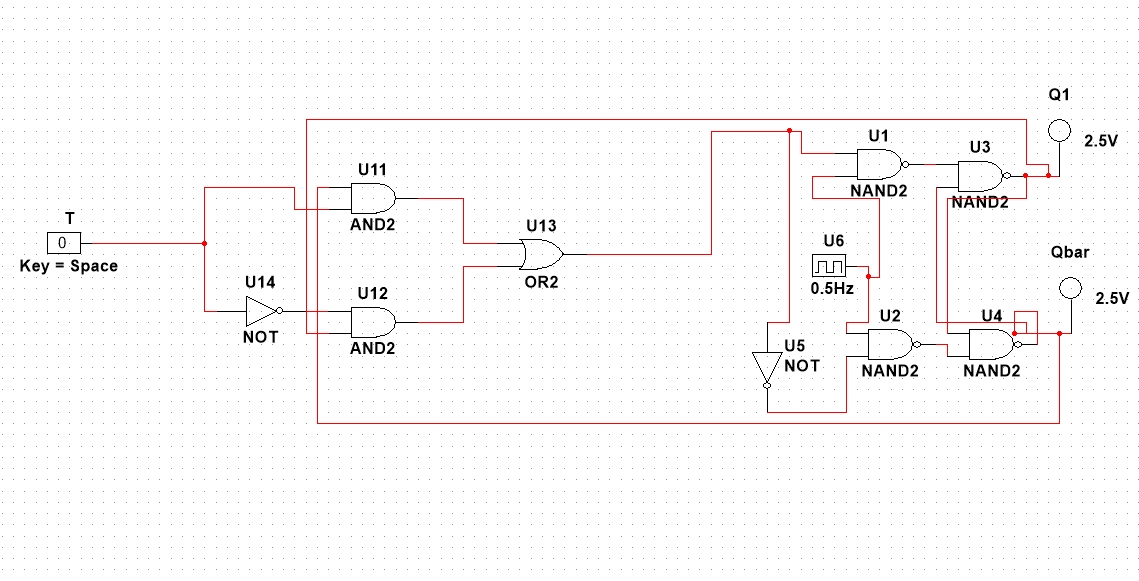


Figure - T FLIP-FLOP

# Discussion:

The experiment was conducted successfully without any major problem. However, as the experiment was mainly conducted online due to precarious circumstances; a few difficulties were faced when trying to identify the different components. The Flip-Flops were designed mainly using their logic gate counterparts and this played a significant role in ensuring that the concept was understood properly. A problem was identified when designing the T Flip-Flop when despite following the “T-shaped” semantics, the circuit was not functioning properly. However, that was solved when the connections between the input and the AND gates were fixed.